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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/709,594	05/17/2004	Jia-Bin Huang	REAP0063USA	3593
27765	7590	01/11/2008		
NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION P.O. BOX 506 MERRIFIELD, VA 22116			EXAMINER SINKANTARAKORN, PAWARIS	
			ART UNIT 2616	PAPER NUMBER
			NOTIFICATION DATE 01/11/2008	DELIVERY MODE ELECTRONIC

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

winstonhsu.uspto@gmail.com  
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<b>Office Action Summary</b>	<b>Application No.</b> 10/709,594	<b>Applicant(s)</b> HUANG, JIA-BIN	
	<b>Examiner</b> Pao Sinkantarakorn	<b>Art Unit</b> 2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 18 October 2007.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)                                | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                       | 5) <input type="checkbox"/> Notice of Informal Patent Application                       |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## **DETAILED ACTION**

### ***Response to Arguments***

1. Applicant's arguments, see page 1, filed 10/18/2007, with respect to the rejection(s) of claim(s) 1, 11, and 18 under 102(e) rejection have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of newly found prior art.
2. Claims 1-20 are currently pending in the application. Claims 19 and 20 have been newly added.

### ***Claim Rejections - 35 USC § 102***

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 5-8, 10-15, 17, 19, and 20 are rejected under 35 U.S.C. 102(e) as being anticipated by Aimoto (newly cited US 6,570,876).

**Regarding claims 1 and 11**, Aimoto discloses an apparatus for improving the management of received data packets of a host system that comprises a plurality of

data buffers and a plurality of descriptors that corresponds to a subset of the plurality of data buffers to manage the received data packets, the apparatus comprising:

a receiver for receiving a data packet (see column 5 lines 23-25);

a first storage unit for storing the data packet from the receiver (see column 3 lines 25-27);

a counter for monitoring the number of descriptors in a first state to produce a count value (see Figure 1 reference numeral 81, column 3 lines 49-56, and column 10 lines 30-35, a counter area for counting the total packet length associated with one of the queue groups);

a second storage unit for storing a threshold value (see column 3 lines 39-40, management table defining a threshold value); and

a comparator for comparing the count value with the threshold value and producing a comparison signal (see column 3 lines 49-56);

wherein the apparatus issues a first event to the host system according to the comparison signal (see column 3 lines 49-56);

**regarding claims 5 and 12**, the first state is an unavailable state (see column 5 lines 50-64);

**regarding claims 6 and 13**, the threshold value is programmable (see column 3 lines 39-40);

**regarding claims 7 and 14**, the first state is a free state (see column 3 lines 49-56);

**regarding claims 8 and 15**, the apparatus issues a second event when the data packet is an ok packet (see column 3 lines 49-56);

**regarding claim 10**, the apparatus is a wireless network device (see column 13 line 41);

**regarding claim 17**, the amount of the descriptors in the first state is monitored when a plurality of error data packets are continuously received (see column 3 lines 49-56, error data packets being the packets in the queue group that has an initial value exceeding its threshold value);

**regarding claim 19**, further comprising  
a masking circuit, for blocking an error signal which indicates the data packet is an error data packet until the count value reaches the threshold value (see column 3 lines 49-56);

**regarding claim 20**, the counter monitors the number of the descriptors in the first state to produce the count value when the apparatus continuously receives a plurality of error data packets; the counter is reset when the data packet is an ok data packet (see column 3 lines 49-56).

***Claim Rejections - 35 USC § 103***

3. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 2 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aimoto in view of Tsujimoto (US 6,700,887).

**Regarding claims 2 and 3**, Aimoto discloses all the subject matter of the claimed invention except the apparatus comprising a Receive DMA (Direct Memory Address) for transferring the data packet from the first storage unit into the data buffers. However, the invention of Tsujimoto from the same or similar fields of endeavor discloses a packet transfer apparatus comprising a DMA controller for controlling a DMA operation between the memory and the buffer (see abstract).

Thus, it would have been obvious to the person of ordinary skill in the art at the time of the invention to implement a packet transfer apparatus comprising a DMA controller for controlling a DMA operation between the memory and the buffer as taught by Tsujimoto into the buffer management apparatus of Aimoto.

The motivation for implementing a packet transfer apparatus comprising a DMA controller for controlling a DMA operation between the memory and the buffer is that it increases the efficiency of the buffer management apparatus.

7. Claims 4, 9, 16, and 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Aimoto in view of Kataria (US 7,177,279).

**Regarding claim 18**, Aimoto discloses a method for improving the management of data packets received from a network by a host system that comprises a plurality of data buffers and that utilizes a plurality of descriptors that corresponds to a subset of the plurality of data buffers to manage the data packets received from the network, the method comprising:

receiving a data packet from the network (see column 5 lines 23-25);

transferring the data packet into at least one of the data buffers (see column 3 lines 25-27);

monitoring the number of descriptors that will have their state changed when the data packet is transferred (see Figure 1 reference numeral 81, column 3 lines 49-56, and column 10 lines 30-35, a counter area for counting the total packet length associated with one of the queue groups);

calculating a count value according to the number of descriptors that will have had their state changed by the data packet being transferred (see Figure 1 reference numeral 81, column 3 lines 49-56, and column 10 lines 30-35, a counter area for counting the total packet length associated with one of the queue groups); and

comparing the count value with the threshold value, and triggering a first event to the host system when the count value reaches the threshold value (see column 3 lines 49-56).

Aimoto fails to disclose an apparatus, wherein the first event notifies the host system to clear the data buffers corresponding to the descriptors. However, the invention of Kataria from the same or similar field of endeavors discloses an apparatus, wherein the first event notifies the host system to clear the data buffers corresponding to the descriptors (see column 5 lines 10-18, column 6 lines 11-16 and lines 47-60, buffer controller generates signals to cell admission interface to flush reassembly buffers and drop all subsequent cells).



Thus, it would have been obvious to the person of ordinary skill in the art at the time of the invention to implement an apparatus, wherein the first event notifies the host system to clear the data buffers corresponding to the descriptors as taught by Kataria into the apparatus of Aimoto.

The motivation for implementing an apparatus, wherein the first event notifies the host system to clear the data buffers corresponding to the descriptors is that it increases the capacity and efficiency of the apparatus.

**Regarding claims 4, 9, and 16**, Aimoto discloses all subject matter of the claimed invention except an apparatus, wherein the first event notifies the host system to clear the data buffers corresponding to the descriptors. However, the invention of Kataria from the same or similar field of endeavors discloses an apparatus, wherein the first event notifies the host system to clear the data buffers corresponding to the descriptors (see column 5 lines 10-18, column 6 lines 11-16 and lines 47-60, buffer controller generates signals to cell admission interface to flush reassembly buffers and drop all subsequent cells).

Thus, it would have been obvious to the person of ordinary skill in the art at the time of the invention to implement an apparatus, wherein the first event notifies the host system to clear the data buffers corresponding to the descriptors as taught by Kataria into the apparatus of Aimoto.

The motivation for implementing an apparatus, wherein the first event notifies the host system to clear the data buffers corresponding to the descriptors is that it increases the capacity and efficiency of the apparatus.

### ***Conclusion***

8. Examiner's Note: Examiner has cited particular columns and line numbers in the references applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings of the art and are applied to specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant in preparing responses, to fully consider the references in entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the Examiner.

In the case of amending the claimed invention, Applicant is respectfully requested to indicate the portion(s) of the specification which dictate(s) the structure relied on for proper interpretation and also to verify and ascertain the metes and bounds of the claimed invention.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pao Sinkantarakorn whose telephone number is 571-270-1424. The examiner can normally be reached on Monday-Thursday 9:00am-3:00pm EST.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ricky Ngo can be reached on 571-272-3139. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

PS



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SUPERVISORY PATENT EXAMINER